



NovaUCD

## Technology Transfer Opportunity

### High-rate LDPC Codes for Data Storage Applications

#### OPPORTUNITY:

High-rate LDPC codes for data storage applications.

#### Description of Technology:

Correcting for errors in digital data transmission is a key challenge in the error-tolerant communication and digital storage technologies.

Based on an idea from finite geometry, this structured LDPC code has a Tanner graph of large girth, enabling superior error suppressing performance at high S/N ratio compared to currently available error-correcting schemes.

#### Value Proposition:

This novel approach to error correction offers key advantages over currently available solutions:

- This code enables state-of-the-art low error frequency at high S/N Ratios (10<sup>-8</sup> bit error rate at S/N of 4.01)
- Compared to traditional pseudo-random LDPC codes, this technology is simpler to implement due to its structured design
- Compared to Turbo codes, it offers low decoding latency, and is therefore highly compatible with high data rate communication systems and high-density magnetic storage systems

#### Market:

Magnetic storage technologies. Companies involved with digital data storage technology might be interested in the error correcting codes introduced herein.

#### Inventors:

Dr Marcus Greferath and Ms Cornelia Roessing, UCD School of Mathematical Sciences, and Dr Mark Flanagan, UCD School of Electrical, Electronic and Mechanical Engineering.

#### Publications:

M. Flanagan, M. Greferath, and C. Roessing: On LDPC Codes from (0,1)-Geometries induced by Finite Inversive Spaces of Even Order. Proceedings of WCC-2007, Versailles, France (2007).

#### Status:

A priority patent application was filed on April 13th 2007 at the Irish Patent Office. PCT application is pending. Validation of the technology in extended S/N Ratio scenarios is on-going.

#### Opportunity Sought:

Relevant industrial partners are sought for licensing and accelerated validation of the technology.

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